Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A test method of a memory IC function, comprising:

preparing a memory tester;

preparing memory ICs of different types;

transmitting data related to each test method of the memory ICs to the memory tester;

generating a random number indicative of a period of time;

executing a test of a predetermined memory IC for the period of time in accordance with the generated random number;

judging whether tests of all the memory ICs are finished or not;

repeating said generating a random number and said executing a test if tests of all the memory ICs are not finished; and

ending processing if tests of all the memory ICs are finished.

Claim 2 (Previously Presented): The test method of a memory IC function, according to Claim 1, wherein the random number is an arbitrary integer from 0 to 255.

Claim 3 (Currently Amended): The test method of a memory IC function, according to Claim 1, wherein the memory ICs include Flash ROM, SRAM [[DRAM]], and SDRAM.

Claim 4 (Previously Presented): The test method of a memory IC function, according to Claim 1, further comprising performing timer interruption processing after said executing a test.

Claim 5 (Original): The test method of a memory IC function, according to Claim 4, wherein the timer interruption processing is performed with a predetermined cycle.

Claim 6 (Previously Presented): The test method of a memory IC function, according to Claim 5, wherein the predetermined cycle is in a range of milliseconds.

Claim 7 (Canceled)

Claim 8 (Previously Presented): The test method of a memory IC function, according to Claim 10, wherein the random number is an arbitrary integer from 0 to 255.

Claim 9 (Canceled)

Claim 10 (Currently Amended): A test method of a memory IC function, comprising:

preparing a memory tester;

preparing ICs of different types;

transmitting data related to each test method of the ICs to the memory tester;

generating a random number;

executing a test of a predetermined IC based on the generated random number;

judging whether tests of all the ICs are finished or not;

repeating said generating a random number and said executing a test if tests of all the ICs are not finished; and

ending processing if tests of all the ICs are finished,

wherein the ICs include a memory IC, a communication interface IC, and a CPU peripheral IC, and wherein the memory IC includes Flash ROM, SRAM [[DRAM]], and SDRAM.

Claim 11 (Previously Presented): The test method of a memory IC function, according to Claim 10, wherein the communication interface IC is an IC including a UART interface and a universal serial bus interface.

Claim 12 (Previously Presented): A test method of a memory IC function, comprising:

preparing a memory tester;

preparing ICs of different types;

transmitting data related to each test method of the ICs to the memory tester;

generating a random number;

executing a test of a predetermined IC based on the generated random number;

judging whether tests of all the ICs are finished or not;

repeating said generating a random number and said executing a test if tests of all the ICs are not finished; and

ending processing if tests of all the ICs are finished,

wherein the ICs include a memory IC, a communication interface IC, and a CPU peripheral IC, and wherein the CPU peripheral IC is an IC including DMAC.

Claim 13 (Previously Presented): The test method of a memory IC function, according to Claim 10, further comprising performing timer interruption processing after said executing a test.

Claim 14 (Previously Presented): The test method of a memory IC function, according to Claim 13, wherein the timer interruption processing is performed with a predetermined cycle.

Claim 15 (Previously Presented): The test method of a memory IC function, according to claim 14, wherein the predetermined cycle is in a range of milliseconds.

Claim 16 (Previously Presented): The test method of a memory IC function, according

to Claim 12, wherein the random number is an arbitrary integer from 0 to 255.

Claim 17 (Previously Presented): The test method of a memory IC function, according to Claim 12, wherein the communication interface IC is an IC including a UART interface and a universal serial bus interface.

Claim 18 (Previously Presented): The test method of a memory IC function, according to Claim 12, further comprising performing timer interruption processing after said executing a test.

Claim 19 (Previously Presented): The test method of a memory IC function, according to Claim 18, wherein the timer interruption processing is performed with a predetermined cycle.

Claim 20 (Previously Presented): The test method of a memory IC function, according to claim 19, wherein the predetermined cycle is in a range of milliseconds.